REMARKS

Reconsideration of this application is respectfully requested. Claim 1 has been amended to correct a clerical error. Claims 16, 25, 31 and 33 have been canceled. Claims 26-30, 32, 34 and 35 have been withdrawn from consideration. No new matter has been added. Claims 1-15, 17-24, 26-30, 32, 34 and 35 remain pending.

Claim Rejections – 35 U.S.C. § 112

Claims 1-14 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite, because "the AB logic operation," as recited in claim 1, lacks clear antecedent basis since there are a plurality of logic operations.

Applicant has amended "the result of the AB logic operation," on line 6 of claim 1, to read "the results of the AB logic operations," and therefore submits that the rejections of claims 1-14 are overcome. Applicant notes that these amendments do not narrow the scope of the claims, and therefore are not narrowing amendments.

Claim Rejections – 35 U.S.C. § 102

Claim 1 has been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,808,927 to Hesson et al. ("Hesson"). Applicant respectfully disagrees with the reasons for rejection.

Claim 1 recites, in part:

> switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the results of the AB logic operations.

Hesson discloses a full adder circuit comprising two exclusive-OR (XOR) circuits (41 and 42), wherein the first XOR circuit (41) "receives inputs A, $\overline{A}$, B, and $\overline{B}$ and outputs $A \bullet \overline{B} + \overline{A} \bullet B$ (i.e. XOR) and $A \bullet B + \overline{A} \bullet \overline{B}$ (i.e. $\overline{XOR}$)." The second XOR circuit (42), identical to the first, receives the XOR and $\overline{XOR}$ outputs of the first XOR circuit (41) at it's A and $\overline{A}$ inputs, respectively, and receives CIN and $\overline{CIN}$ at its B and $\overline{B}$ inputs, respectively (Hesson, Fig. 4, col. 5 lines 57-59 and col. 6 lines 31-34). Thus, applicant submits that the XOR circuits do not

independently generate the logic operations $A \bullet \overline{B}$ or $\overline{A} \bullet B$, but rather a single operation (XOR) that is a logical combination of the two. Applicant further submits that neither the XOR (i.e. $A \bullet \overline{B} + \overline{A} \bullet B$) output, nor the $\overline{XOR}$ (i.e. $A \bullet B + \overline{A} \bullet \overline{B}$) output, of the first XOR circuit is an "AB logic operation," as recited in claim 1. Thus, even assuming arguendo that the second XOR circuit of Hesson corresponds to the switch circuitry of applicant's claim 1, as suggested in the Office Action, Hesson still does not disclose "switch circuitry coupled to the control logic to receive a result of *the AB logic operation* from each of the plurality of logic cells," as recited in claim 1, but rather discloses that the second XOR circuit receives $A \bullet \overline{B} + \overline{A} \bullet B$ (i.e. XOR) and $A \bullet B + \overline{A} \bullet \overline{B}$ (i.e. $\overline{XOR}$) logic operations from the first XOR circuit.

Further, assuming arguendo that the second XOR circuit of Hesson corresponds to the switch circuitry of applicant's claim 1, as suggested in the Office Action, Hesson still does not disclose "switch circuitry coupled to the control logic to receive a result of the AB logic operation *from each of the plurality of logic cells*," as recited in claim 1. In contrast, Hesson's second XOR circuit receives the XOR and $\overline{XOR}$ outputs only from the *first XOR circuit*, and therefore is not a switch circuitry as recited in Applicant's claim 1.

For at least the reasons given above in reference to claim 1, applicant submits that Hesson does not disclose at least the above-recited limitations of claim 1. Therefore, Hesson does not anticipate claim 1.

Claim Rejections – 35 U.S.C. § 103

Claim 1 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,479,112 to Choi et al. ("Choi"). Applicant respectfully disagrees with the reasons for rejection.

Claim 1 recites, in part:

> switch circuitry coupled to receive input data, the switch circuitry coupled to the control logic to receive a result of the AB logic operation from each of the plurality of logic cells and selectively enable the output of one or more bits of the input data based on the results of the AB logic operations.

Choi discloses a CMOS differential exclusive-OR (XOR) gate (8) having an XOR circuit (10) and an $\overline{XOR}$ circuit (12), wherein "the XOR circuit 10 produces an output OUTP which is

the logical XOR of the input signals A and B," and wherein "the $\overline{XOR}$ circuit operates to produce an output (OUTM) which is $\overline{XOR}$ of input signals A and B" (Choi, Fig. 1, col. 5 line 50 to col. 6 line 4). However, nowhere does Choi suggest or disclose "switch circuitry coupled to receive input data," as recited in claim 1, nor is any such disclosure pointed out in the Office Action. Furthermore, the output OUTP of the exclusive-OR gate represents the logic operation: $(A \bullet \overline{B} + \overline{A} \bullet B)$, and the output OUTM represents the logic operation: $A \bullet B + \overline{A} \bullet \overline{B}$ (Choi, col. 5 lines 56-57 and col. 6 lines 2-3). Thus, applicant submits that the $\overline{XOR}$ circuit does not independently generate the logic operation, $A \bullet B$.

Even assuming arguendo that the exclusive-OR gate of Choi corresponds to the control logic of applicant's claim 1, as suggested in the Office Action, there still would have been no motivation to include "switch circuitry coupled to the control logic to receive a result of *the AB logic operation* from each of the plurality of logic cells," as recited in claim 1, since the exclusive-OR gate does not output a plurality of AB logic operations, but rather outputs the single logical combination: $A \bullet B + \overline{A} \bullet \overline{B}$. Therefore, because Choi does not disclose outputting a plurality of AB logic operations, there is no reason to modify Choi to include switch circuitry that receives and switches between input data, based on the plurality of AB logic operations, as recited in Applicant's claim 1. Accordingly, the Office Action has not made a prima facie case of obviousness under 35 U.S.C. § 103.

Claims 2-14 depend from claim 1 and therefore distinguish over the cited references for at least the same reasons as claim 1.

Allowable Subject Matter

Applicant respectfully acknowledges that claims 15 and 17-24 have been allowed, and notes that claims 2-14 would be allowable if re-written in independent form to include the limitations of the rejected base claim and any intervening claims.

Conclusion

In light of the above remarks, it is believed that pending claims 1-15, 17-24 are in condition for allowance and, therefore, a Notice of Allowance of claims 1-15, 17-24 is respectfully requested. If a telephone interview would be helpful in any way, the Examiner is invited to call the undersigned agent.

Applicant hereby petitions for a 2 month extension of time

Authorization is hereby given to charge deposit account 501914 for any fee due in connection with this Amendment, including any fee due in connection with a petition for extension of time.

Respectfully submitted,
SHEMWELL MAHAMEDI LLP

Date February 21, 2008

Yipeng Li, Reg. No. 60,595
Tel. 408-236-6638